

REMARKS

Following entry of the above amendment, claims 1-14 and 22-27 will be pending. Claims 15-21 have been cancelled without prejudice or disclaimer.

I. AMENDMENTS TO THE CLAIMS

Claim 9 has been amended to provide proper antecedent basis for the term “first semiconductor material,” without change of scope. Specifically, the term “device layer semiconductor” has been replaced with the term “first semiconductor material”. Further, the amendments to claim 9 are not substantive to the claims and do not raise new issues of patentability.

II. DRAWINGS

Formal drawings are submitted herewith. As discussed above, the formal drawings include amendments to clearly identify each referenced feature. This, along with corresponding changes in the specification, cures the use of reference numerals with regard to more than one feature, for example. No new matter has been added.

III. AMENDMENTS TO THE SPECIFICATION

The Applicants have amended the disclosure to correct informalities. For example, the reference numeral “22” has been changed to “94” when used to identify the backgate. Further, amendments have been made to consistently identify the silicon device layer 26, the buried oxide layer 72, the channel region 92, the backgate 94 and the steps of the method of fabricating the semiconductor device. No new matter has been added.

IV. REJECTION OF CLAIMS UNDER 35 USC §102(b)

Claims 1-14 and 22-27 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Thapar et al., U.S. Patent No. 5,753,938 (“Thapar”). Withdrawal of the rejection is respectfully requested for at least the following reasons.

Thapar describes a semiconductor switching device. The switching device includes a plurality of heterojunction-gate static-induction transistor unit cells in a monocrystalline silicon carbide substrate. (See, e.g., Abs, Ins. 1-4). As is shown in Fig. 1 of Thapar (reproduced below), a drain region 14, a drift region 16 and a source region 20 are made of **silicon carbide**. (See, e.g., Abs, Ins. 5-9, Col. 4, ln. 60- Col. 5, ln. 5). The gate regions 28 are made of a nonmonocrystalline silicon, i.e., a material selected from the group consisting of polycrystalline silicon and amorphous silicon. (See, e.g., Col. 5, Ins. 28-33). However, Thapar does not disclose a transistor structure in which a central channel region, a source region and a drain region are of a first semiconductor (material); and a gate, on the other hand, includes a first semiconductor (material) and a second semiconductor with an energy gap **greater** than the first semiconductor (material).

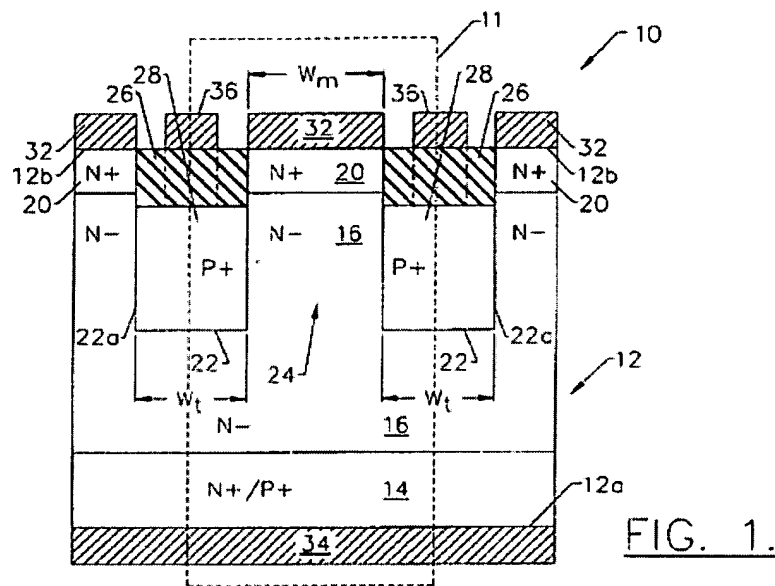


Figure 1 of Thapar et al.

Claim 1 recites a transistor structure that includes, *inter alia*, a central channel region, a source region, and a drain region consisting of a first semiconductor. In addition, the transistor structure has a gate adjacent the channel region. The gate includes the first semiconductor and a second semiconductor with an energy gap **greater** than the first semiconductor. Similarly, claim 8 describes a **silicon on insulator** transistor structure in which the central channel region, the source region and the drain region consist of a first semiconductor material. The gate, on the

other hand, includes the first semiconductor material and a second semiconductor with an energy gap **greater** than the first semiconductor material.

Further, the present application describes the transistor structure as having a silicon device layer 26. Accordingly, the central channel region 14, the source region 16 and the drain region 18 are formed of silicon, for example. Silicon is a first semiconductor (material). (See, e.g., Fig. 1, page 6, lns. 15-19). The gate 34 and the backgate 38, on the other hand, are formed of silicon carbide. That is, the gate 34 and the backgate 38 are formed of the first semiconductor (material) silicon and a second semiconductor, carbon. Thus, the gate 34 and the backgate 38 in the transistor structure of the present invention are made of **a first semiconductor (material) and a second semiconductor** with an energy gap **greater** than the first semiconductor (material) alone of the central channel region 14.

The Examiner contends Thapar teaches all of the features of claim 1 and claim 8 citing the Abs., lines 1-25 and Col. 6-7, lines 65-8 and the Abs., lines 1-25 and Col. 6-7, lines 65-8, Col. 3, lines 1-10, Col. 5, lines 60-68, and Col. 2, lines 50-60, respectively. Further, the Examiner contends Thapar discloses a gate consisting of two different materials having two different energy gap dimensions. The Examiner supports this conclusion by stating the silicon carbide layer 116 as illustrated in Figures 3E and 3F is formed directly beneath gate 128 and can therefore be interpreted to be part of the gate region. First, the silicon carbide layer 116 is not part of the gate as clearly illustrated and disclosed by Thapar. Thapar discloses the gate 28 of nonmonocrystalline silicon forms rectifying P-N junctions with the silicon carbide drift region 16 (drift region 16 corresponds to drift region 116) at the sidewalls 22a and bottoms of the trenches 22. (See, e.g., Col. 5, lines 33-37). Thus, the drift region 16 consists of two different materials and the gate 28 consists of a single material. The single material of gate 28 has an energy gap **less** than the energy gap of the drift region 16 which consists of two different materials.

Further, Thapar does not disclose a transistor structure in which a central channel region, a source region and a drain region are of a first semiconductor (material); and a gate, on the other hand, includes a first semiconductor (material) and a second semiconductor with an energy gap **greater** than the first semiconductor (material). To the contrary, Thapar discloses directly opposite the invention recited in claims 1 and 8. Thapar discloses that the drift region 16, the

source region 20 and the drain region 14 are made of a first semiconductor and a second semiconductor having an energy gap **greater** than the first semiconductor from which the gates 28 are made. Additionally, Thapar discloses silicon carbide may be considered for the gate region material provided a wide bandgap material used to form the drift region has a sufficiently large bandgap energy. (See, e.g., Col. 7, lns. 4-8).

The present invention, on the other hand, calls for a **gate made of a first semiconductor (material) and a second semiconductor** having an energy gap **greater** than the **first semiconductor (material)** from which the central channel region, source region and drain region are made. Further with regard to claim 8, Thapar does not disclose an SOI substrate. Thapar discloses an insulating layer may be provided on the nonmonocrystalline gate regions to isolate the gate regions from **metallization** on the second face. (See, e.g., Col. 3, lns. 4-7). Since, Thapar does not teach each and every feature of the invention, claims 1-14 and 22-27 are patentable over Thapar.

In addition to the reasons recited above in connection with claims 1 and 8 from which they depend, the remaining claims may be distinguished over Thapar based on the particular features recited therein.

For example, claims 3, 4, 10 and 11 specifically recite the composition of the gate and channel regions. Such construction is directly opposite the teachings of Thapar.

Claims 24 and 27 refer to a conductive via electrically coupling the gate to a backgate. Thapar simply does not teach or suggest any such conductive via.

Claim 25 refers to the gate extending the entire length of the channel region between the source region and the drain region. There is no such gate in Thapar extending the entire length between the source 20 and drain 14.

V. CONCLUSION


In light of the foregoing, it is respectfully submitted that the present application is in condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in condition for allowance, the Examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present invention.

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Attorney Docket No. F0588
Firm Reference No. AMDSP0480US

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Any fee(s) resulting from this communication is hereby authorized to be charged to our
Deposit Account No. 18-0988; Our Order No. F0588 (AMDSP0480US).

Respectfully submitted,
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